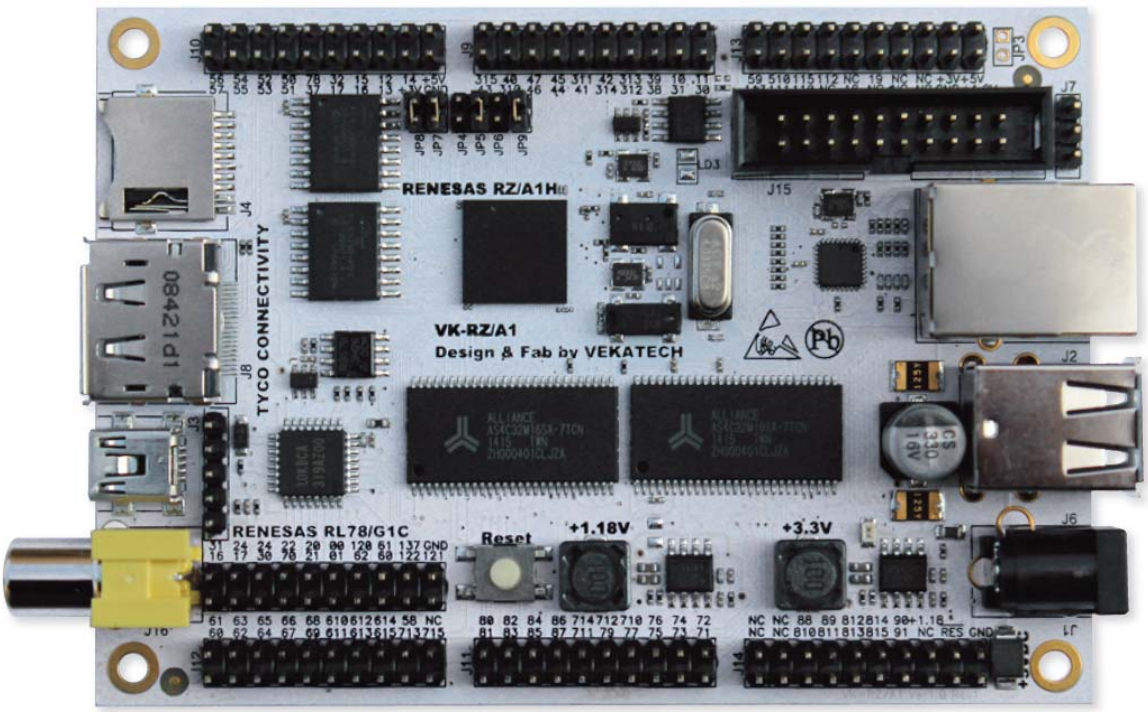
VK-RZ/A1H Development Board
V3.0
User manual



Rev. 3.0, Sep.18.2015

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INTRODUCTION

VK-RZ/A1 is a development board which uses MCU R7S721000VCBG from Renesas Electronics. This powerful MCU is actually LSI, single-chip microcontroller that includes an ARM Cortex™-A9 processor along with the integrated peripheral functions required to configure a system. The core includes:

- 32-KB L1 instruction cache
- 32-KB L1 data cache
- 128-KB L2 cache.

Integrated various on-chip peripheral functions and interfaces such as:

- 10-MB large-capacity RAM (128 KB are shared by the data-retention RAM)
- data-retention RAM
- multi-function timer pulse unit 2, OS timer, realtime clock
- motor control PWM timer
- UART, UART with FIFO, I2C, SPI, SPI multi I/O bus controller, CAN, LIN
- serial sound interface, sound generator, CD-ROM decoder
- A/D converter, SCUX
- media local bus, SD host interface, MMC host interface
- NAND flash memory controller
- IEBus™ controller, Renesas SPDIF interface
- Ethernet controller, EthernetAVB
- USB 2.0 host/function
- digital video decoder, video display controller 5
- dynamic range compression, image renderer, image renderer for display
- display out comparison unit
- Renesas graphics processor for OpenVG™
- JPEG codec unit, capture engine unit, pixel format converter
- interrupt controller modules, general I/O ports

The kit supports:

- CAN
- Ethernet
- LVDS Port (optional)
- up to 128 MB SDRAM
- up to 640 MB SPI Flash
- I^2C RTC, I^2C Crypto Auth. (optional)
- Mini SD card connector
- Composite video connector (optional)
- USB ↔ UART converter
- 2 USB communication channels

All this along with the DC/DC power supply on board and connected to pin headers unused pins of R5F10KBC & R7S721000VCBG allow you to build a diversity of powerful applications to be used in a wide range of embedded tasks.

BOARD FEATURES:

- MCU: RL78/G1C - (R5F10KBC)
- LSI: RZ/A1H - (R7S721000VCBG)
- USB Mini B device connector (RL78/G1C)
- 2xUSB Standard A host connectors (RZ/A1H)
- Micro SD card connector (RZ/A1H)
- Composite video connector (RZ/A1H)
- LVDS Port connector (RZ/A1H)
- CAN connectors (NXP TJA1040) - (RZ/A1H)
- RJ-45 ethernet connector 10/100Mb MAC (PHY SMSC LAN8710A) - (RZ/A1H)
- SDRAM 32 MB (CS2, 64MB per chip select) - (RZ/A1H)
- 4 bit SPI Flash (2x16 Mbits Spansion S25FL128S) - (RZ/A1H)
- I^2C RTC with battery holder (ST M41T82) - (RZ/A1H)
- I^2C Crypto Authentication (Atmel ATSHA204) - (RZ/A1H)
- 20 pins Debug/programming connector (JTAG)
- 5 pin Debug/programming Emulator connector (Renesas E1)
- Power connector for DC/DC (In: 5V → Out: 3V3 & 1V18)
- FR-4, 2.0 mm, Orange/Blue/Red solder mask, component print
- Dimensions: 105.0mm x 74.0mm

ELECTROSTATIC WARNING

The VK-RZ/A1H - R7S721000VCBG board is shipped in protective anti-static packaging. The board must not be subject to high electrostatic potentials. General practice for working with static sensitive devices should be applied when working with this board.

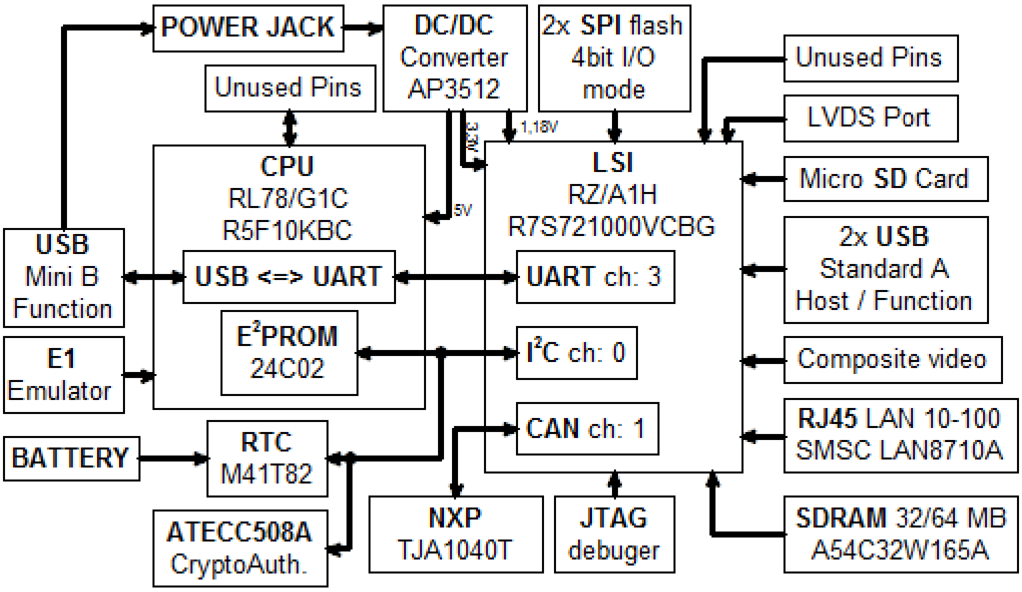
PROCESSOR FEATURES

The VK-RZ/A1H board use MCU R7S721000VCBG from RENESAS ELECTRONICS
with these features:

- Power supply voltage: VDD = 3.0 to 3.6 V
- Operating ambient temperature: TA =−40 to +85°C
- Max. CPU clock (Iϕ) = 400 MHz)

For more information please visit www.renesas.eu

BLOCK DIAGRAM



EXTERNAL SDRAM BASE ADDRESSES

```
SDRAM CS2:         ORIGIN = 0x08000000,    LENGTH = 64MB
SDRAM CS3:         ORIGIN = 0x0C000000,    LENGTH = 64MB
SDRAM CS2 mirror:  ORIGIN = 0x48000000,    LENGTH = 64MB
SDRAM CS3 mirror:  ORIGIN = 0x4C000000,    LENGTH = 64MB
```

⚠ SDRAM is accessed with 16bit data width

⚠ A14 & A15 are used for bank switching

SCHEMATICS

Please refer to CD for high quality pictures.

POWER SUPPLY CIRCUIT:

VK-RZ/A1H is powered by (5) VDC applied at the power jack.
VK-RZ/A1H could also be powered by USB Mini B connector.
The consumption of VK-RZ/A1H may vary and the maximum is (@3.3V) 450mA.

CLOCK CIRCUITS:

Quartz Generator 13.3333 MHz is connected to **EXTAL,** pin# **AA14**.
Quartz crystal 32.768KHz is connected to **RTC_X1/RTC_X2,** pins# **AA7/Y7**.
Quartz crystal 4.0000MHz is connected to **RTC_X3/RTC_X4,** pins# **V10/V11**.
Quartz crystal 48.0000MHz is connected to **USB_X1/USB_X2,** pins# **AA13/Y13**.
Quartz crystal 27.0000MHz is connected to **VIDEO_X1/VIDEO_X2,** pins# **W21/V20**.
Quartz crystal 22.5792MHz is connected to **AUDIO_X1/AUDIO_X2,** pins# **V21/U20**.
Quartz crystal 25.0000MHz is connected to Ethernet Phy - **SMSC LAN8710A** – (**XTAL1/XTAL2** pins# **5/4**).
Quartz crystal 32.768KHz is connected to RTC – **M41T82** (**XI**/**XO**, pins# **1/2**).

PUSH BUTTONS

Button#	Function	Signal Name	Pin#
SW1	RESET	RESET	U9

JUMPERS CONFIGURATION (■ **Connected** □ **Disconnected**)

MD_BOOT0 input is connected to '1' (3V3), so only **Boot Mode 3/4/5** are available !

MD_BOOT1 input is connected to **JP1** and **MD_BOOT2** to **JP2**.

MD_CLK input is connected to '0' (GND), so the LSI is clocked from **EXTAL**.

BSCANP input connected to '0' (GND), so the LSI is in normal debug interface mode (i.e. JTAG is connected to **CoreSight debug TAP controller**).

BOOT configuration:

BOOT mode#	JP1,	JP2	Description
3	■	□	Boot from **SPI multi I/O ch0:** [P9_2 - P9_5]
4	□	■	Boot from **SD card ch0:** [P4_10 - P4_15]
5	□	□	Boot from **MMC card ch0:**[P5_10 - P5_15]

Clock settings:

CLK mode#	JP3	Description
MD_CLKS	■	SSCG circuit **OFF**
MD_CLKS	□	SSCG circuit **ON**

CAN Termination:

CAN mode#	JP4	Description
0	■	CAN line **is** terminated
1	□	CAN line **isn't** terminated

EXTERNAL CONNECTORS DESCRIPTION

PWR J1			
Pin#	Signal Name	Pin#	Signal Name
1	+5V	2,3	GND

⚠ The power input should be +(5VDC)

E1 Emulator 5pin connector

E1 J17	
Pin#	Signal Name
1	+5V
2	TOOL
3	RESET
4	TRESET
5	GND

JTAG 20pin connector

JTAG J15			
Pin#	Signal Name	Pin#	Signal Name
1	+3V3	2	+3V3
3	TRST	4	GND
5	TDI/JP0_0	6	GND
7	TMS	8	GND
9	TCK	10	GND
11	-	12	GND
13	TDO/JP0_1	14	GND
15	SRST	16	GND
17	-	18	GND
19	-	20	GND

CAN 3pin connector

CAN J7	
Pin#	Signal Name
1	CAN_L
2	GND
3	CAN_H

CTX1 is connected to **P5_10** pin# **A7** of **R7S721000VCBG**.
CRX1 is connected to **P5_9** pin# **B7** of **R7S721000VCBG**.

Termination Jumper **JP4**.

Ethernet connector RJ45 type: J2

Transformer and integrated LEDS are connected to PHY interface **LAN8710A**.

Respective signals from PHY are connected to MII interface of **R7S721000VCBG.**

USB devices

USB mini B J3			
Pin#	Signal Name	Pin#	Signal Name
1	V_USB1	3	D+
2	D-	5	GND

Pin#4 ID is disconnected.
V_USB1 Output USB device power.
D- is connected to **UDM0,** pin#**23** of **R5F10KBC.**
D+ is connected to **UDP0,** pin#**24** of **R5F10KBC.**

USB standard A J6 (lower)			
Pin#	Signal Name	Pin#	Signal Name
1	+5V	3	D+
2	D-	4	GND

USB standard A J6(upper)			
Pin#	Signal Name	Pin#	Signal Name
5	+5V	7	D+
6	D-	8	GND

Both USB are configured as hosts !
lower D- is connected to **DM1,** pin#**AA9** of **R7S721000VCBG**
lower D+ is connected to **DP1,** pin#**Y9** of **R7S721000VCBG**.
upper D- is connected to **DM0,** pin#**AA11** of **R7S721000VCBG**.
upper D+ is connected to **DP0,** pin#**Y11** of **R7S721000VCBG**.

Micro SD card slot:

Micro SD J4			
Pin#	Signal Name	MCU PIN#	MCU PORT
1	DAT2	F18	P4_15/SD_D2_0
2	CD/DAT3	F17	P4_14/SD_D3_0
3	CMD	G20	P4_13/SD_CMD_0
4	VDD	-	-
5	CLK	H21	P4_12/SD_CLK_0
6	GND	-	-
7	DAT0	G18	P4_11/SD_D0_0

8	DAT1	H20	P4_10/SD_D1_0
9	S1	-	-
10	G1	-	-
11	S2	J21	P4_8/SD_CD_0
12	G2	-	-

Composite video

Composite video J16			
Pin#	Signal Name	Pin#	Signal Name
1	VIN1A	2	GND

LVDS port connector: J8

LVDS port J8			
Pin#	Signal Name	MCU PIN#	MCU PORT
1	ML_LANE_0_+	B9	P5_6/TXOUT0P
2	GND	-	-
3	ML_LANE_0_-	A9	P5_7/TXOUT0M
4	ML_LANE_1_+	D10	P5_4/TXOUT1P
5	GND	-	-
6	ML_LANE_1_-	D9	P5_5/TXOUT1M
7	ML_LANE_2_+	B10	P5_2/TXOUT2P
8	GND	-	-
9	ML_LANE_2_-	A10	P5_3/TXOUT2M
10	AUX_CH_+	B11	P5_0/TXCLKOUTP
11	GND	-	-
12	AUX_CH_-	A11	P5_1/TXCLKOUTM
13	-	-	-
14	-	-	-
15	I2C_SCL_3	E13	P1_6/I2C_SCL_3
16	GND	-	-
17	I2C_SDA_3	D13	P1_7/I2C_SDA_3
18	LVDS_HPD	K1	P7_8/IRQ1
19	GND	-	-
20	+3V3	-	-

The signals, that are coming out from the connector, **ARE NOT DISPLAY PORT SIGNALS**, regardless of the fact that the connector is the same as Display port.

CONFIGURABLE REROUTING

There are function and features that can be enabled or disabled by manually soldering or desoldering components, (mostly resistors). Every component, specified with attribute **DNP** is missing by default. If user wants to enable given purpose, related designator should be soldered and sometimes some other components must be desoldered.

Optionals: solder at your own risk, double check & comply with the schematic !			
Designator#	Sheet	Purpose	Dependence
R2	Jumper & Pull-Ups	clock the PHY from P5_9	Remove R3 or R179
R6	LAN	Some Oscillator need it	-
R114	LVDS	Lane 0 impedance match	-
R115	LVDS	Lane 1 impedance match	-
R116	LVDS	Lane 2 impedance match	-
R117	LVDS	Lane aux impedance match	-
R124	LVDS	10k Pull-down CONFIG1	-
R125	LVDS	10k Pull-down CONFIG2	-
R126	LVDS	Access LCD EEPROM from I^2C0	Remove R122
R127	LVDS	Access LCD EEPROM from I^2C0	Remove R120
R131	Jumper & Pull-Ups	Drive LD1 from P1_5	Remove R132
R133	Jumper & Pull-Ups	Drive LD1 from P8_10	Remove R132
R145	MCU Control	clock LSI from USB_X1	Remove R152
R147	MCU Control	Set debug mode to boundary scan	Remove R153
R171	USB-Serial	Bypass level shifter	Remove U20
R176	USB-Serial	Access RL78 EEPROM from I^2C3	Remove R174
R177	USB-Serial	Access RL78 EEPROM from I^2C3	Remove R175
R194	CAN	Put can transceiver in silent mode	Remove R193
R198	RTC & Crypto	Access RTC & Crypto from I^2C3	Remove R201
R200	RTC & Crypto	Access RTC & Crypto from I^2C3	Remove R199
R210	Memory	Invert SD Card detect signal logic	-
U8	MCU Decoupling	If External Reff. Voltage needed	-

UNUSED PIN HEADERS

PORT extension

J5 (RL78/G1C)			
Pin#	Signal Name	Pin#	Signal Name
1	P16/TI01/TO01/INTP5	2	P31/TI03/TO03/INTP4/PCLBUZ0
3	P17/TI02/TO02	4	P24/ANI4
5	P30/INTP3/SCK00/SCL00 /(TI03/TO03/PCLBUZ0)	6	P23/ANI3
7	P70/PCLBUZ1	8	P22/ANI2
9	P21/ANI1/AV_{REFM}	10	P20/ANI0/AV_{REFP}
11	P01/ANI16/TO00/INTP9 /SCK01/SCL01/(SCLA0)	12	P00/ANI17/TI00/INTP8/SI01 /SDA01/(SDAA0)
13	P62	14	P120/ANI19/SO01/(PCLBUZ1)
15	P60/SCLA0	16	P61/SDAA0
17	P122/X2/EXCLK	18	P137/INTP0
19	P121/X1	20	GND

LCD extension

J9 (RZ/A1H)			
Pin#	Signal Name	Pin#	Signal Name
1	P1_1/RIIC0SDA	2	P3_0/LCD0_CLK
3	P1_0/RIIC0SCL	4	P3_1/LCD0_TCON0 (DE)
5	P3_9/LCD0_DATA1 (B2)	6	P3_8/LCD0_DATA0 (B1)
7	P3_13/LCD0_DATA5 (G0)	8	P3_12/LCD0_DATA4 (B5)
9	P4_2/LCD0_DATA10 (G5)	10	P3_14/LCD0_DATA6 (G1)
11	P3_11/LCD0_DATA3 (B4)	12	P4_1/LCD0_DATA9 (G4)
13	P4_5/LCD0_DATA13 (R3)	14	P4_4/LCD0_DATA12 (R2)
15	P4_7/LCD0_DATA15 (R5)	16	P4_6/LCD0_DATA14 (R4)
17	P4_0/LCD0_DATA8 (G3)	18	P3_10/LCD0_DATA2 (B3)
19	P3_15/LCD0_DATA7 (G2)	20	P4_3/LCD0_DATA11 (R1)

J10 (RZ/A1H)			
Pin#	Signal Name	Pin#	Signal Name
1	+5V	2	GND
3	P1_4/RIIC2SCL	4	+3V3
5	P1_2/RIIC1SCL	6	P1_3/RIIC1SDA
7	P1_5/RIIC2SDA	8	P1_6/RIIC3SCL
9	P3_2/LCD0_TCON1 (Hsync) On/Off	10	P1_7/RIIC3SDA
11	P7_8/IRQ1	12	P3_7/LCD0_TCON6 (Vsync) (BKL_EN)
13	P5_0/TXCLKOUTP	14	P5_1/TXCLKOUTM
15	P5_2/TXOUT2P	16	P5_3/TXOUT2M
17	P5_4/TXOUT1P	18	P5_5/TXOUT1M
19	P5_6/TXOUT0P	20	P5_7/TXOUT0M

SDRAM extension

J11 (RZ/A1H)			
Pin#	Signal Name	Pin#	Signal Name
1	P8_1/A9	2	P8_0/A8
3	P8_3/A11	4	P8_2/A10
5	P8_5/A13	6	P8_4/A12
7	P8_7/A15	8	P8_6/A14
9	P7_11/A3	10	P7_14/A6
11	P7_9/A1	12	P7_12/A4
13	P7_7/WE1/DQMLU	14	P7_10/A2
15	P7_5/RD/WR	16	P7_6/WE0/DQMLL
17	P7_3/CAS	18	P7_4/CKE
19	P7_1/CS3	20	P7_2/RAS

J12 (RZ/A1H)			
Pin#	Signal Name	Pin#	Signal Name
1	P6_1/D1	2	P6_0/D0
3	P6_3/D3	4	P6_2/D2
5	P6_5/D5	6	P6_4/D4
7	P6_7/D7	8	P6_6/D6
9	P6_9/D9	10	P6_8/D8
11	P6_11/D11	12	P6_10/D10
13	P6_13/D13	14	P6_12/D12
15	P6_15/D15	16	P6_14/D14
17	P7_13/A5	18	P5_8/CS2
19	P7_15/A7	20	n.c

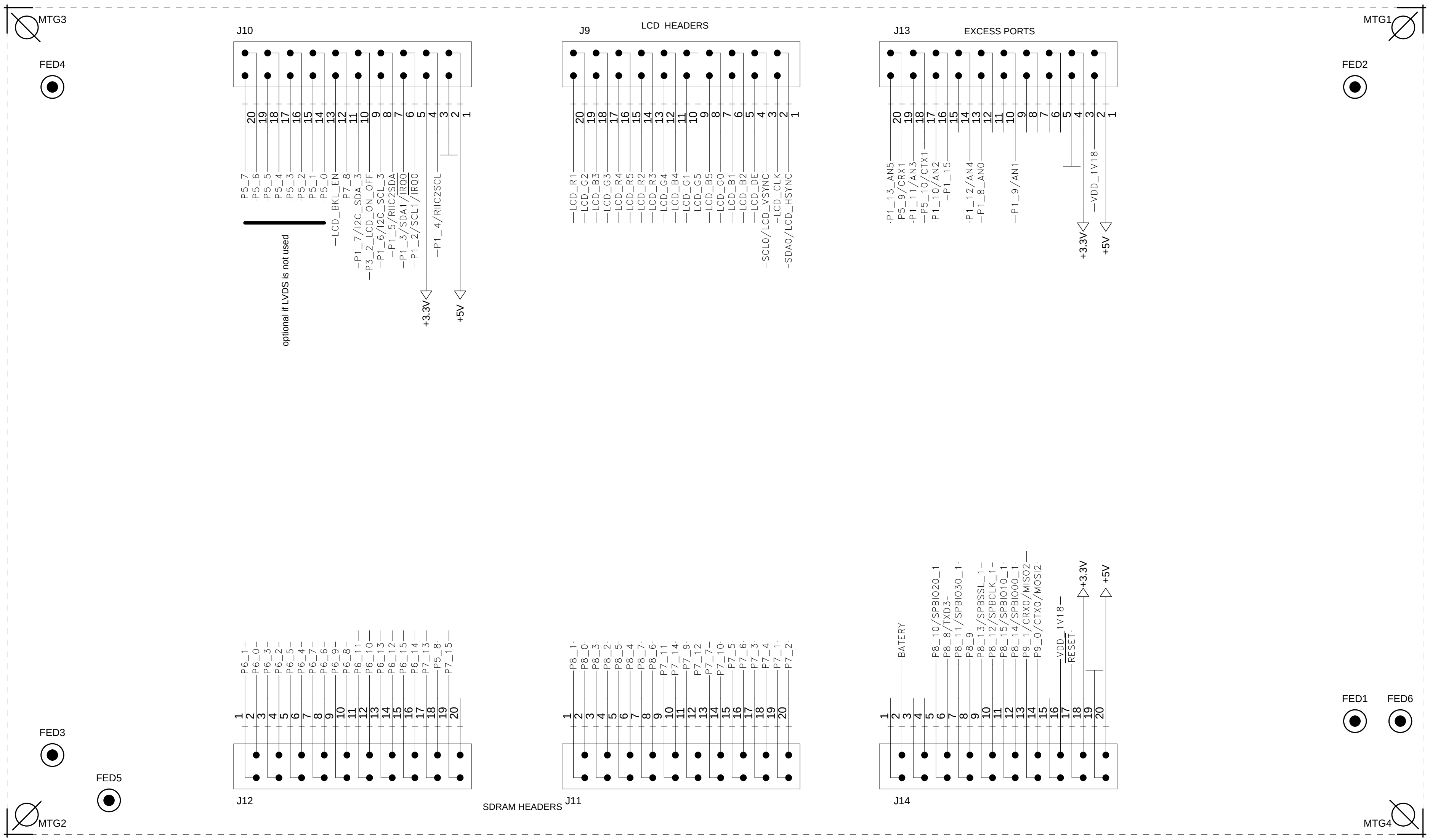
PORT extension

J13 (RZ/A1H)			
Pin#	Signal Name	Pin#	Signal Name
1	+5V	2	+1V18
3	+3V3	4	GND
5	n.c	6	n.c
7	n.c	8	n.c
9	P1_9/AN1	10	n.c
11	n.c	12	P1_8/AN0
13	P1_12/AN4	14	n.c
15	P1_15/AN7	16	P1_10/AN2
17	P5_10/CAN1TX	18	P1_11/AN3
19	P5_9/CAN1RX	20	P1_13/AN5

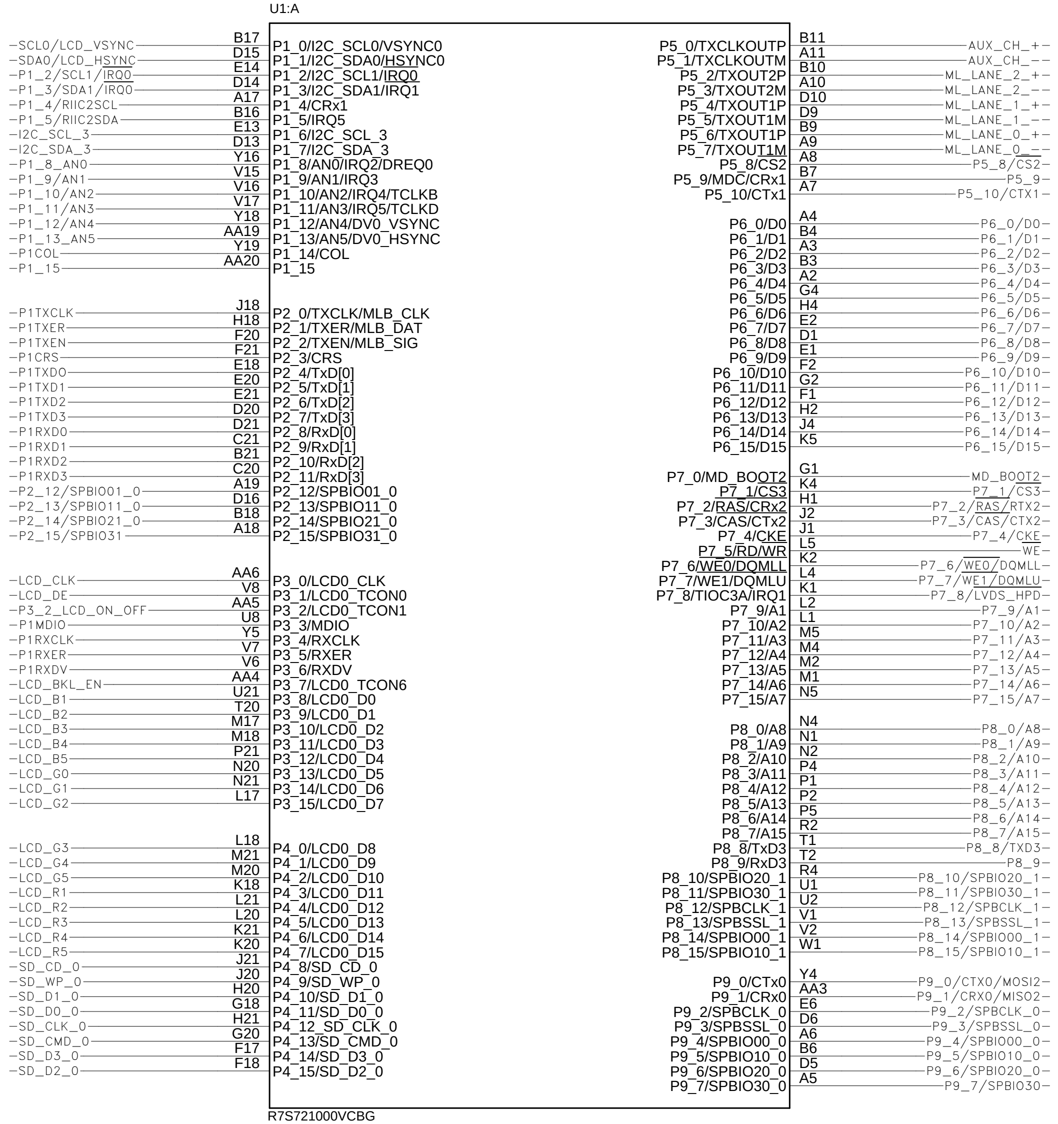
J14 (RZ/A1H)			
Pin#	Signal Name	Pin#	Signal Name
1	n.c	2	Battery
3	n.c	4	n.c
5	P8_10	6	P8_8/TxD3
7	P8_11	8	P8_9/RxD3
9	P8_13	10	P8_12
11	P8_15	12	P8_14
13	P9_1	14	P9_0
15	n.c	16	+1V18
17	RESET	18	+3V3
19	GND	20	+5V

AVAILABLE DEMO SOFTWARE:

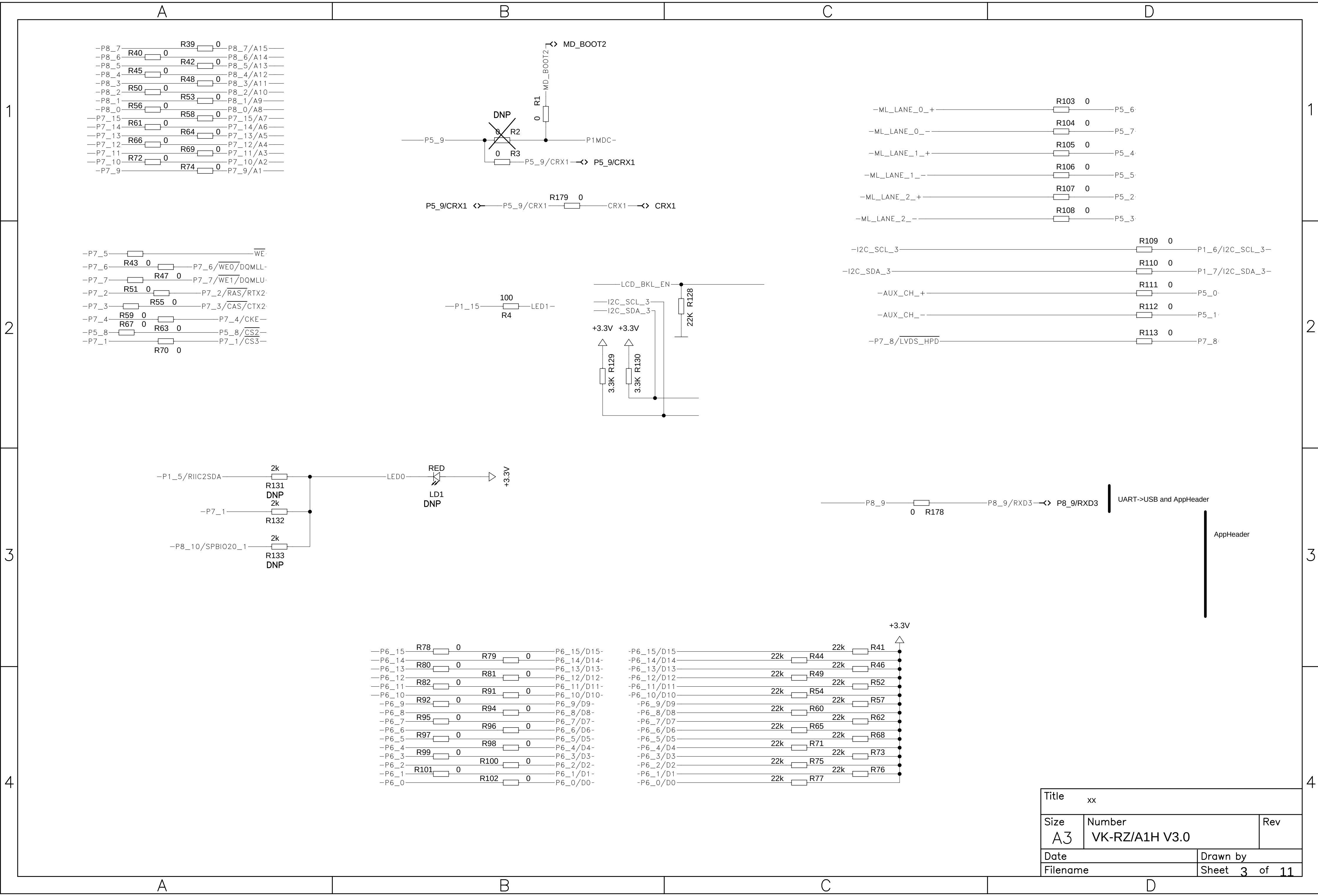
1. FREERTOS(TM) DEMO PROJECT PORTED FOR IAR AND BUILT FOR VK-RZ/A1H development board.
2. CycloneTCP PROJECT PORTED FOR IAR AND BUILT FOR VK-RZ/A1H development board.
3. u-boot, Linux PORTED FOR GCC AND BUILT FOR VK-RZ/A1H development board.
4. Express_Logic_Embedded_GUI demo.
5. IS2S MicroEJ demos.
6. Microsoft Micro .net framework
7. Micro .net framework PORTED FOR VK-RZ/A1H development board.



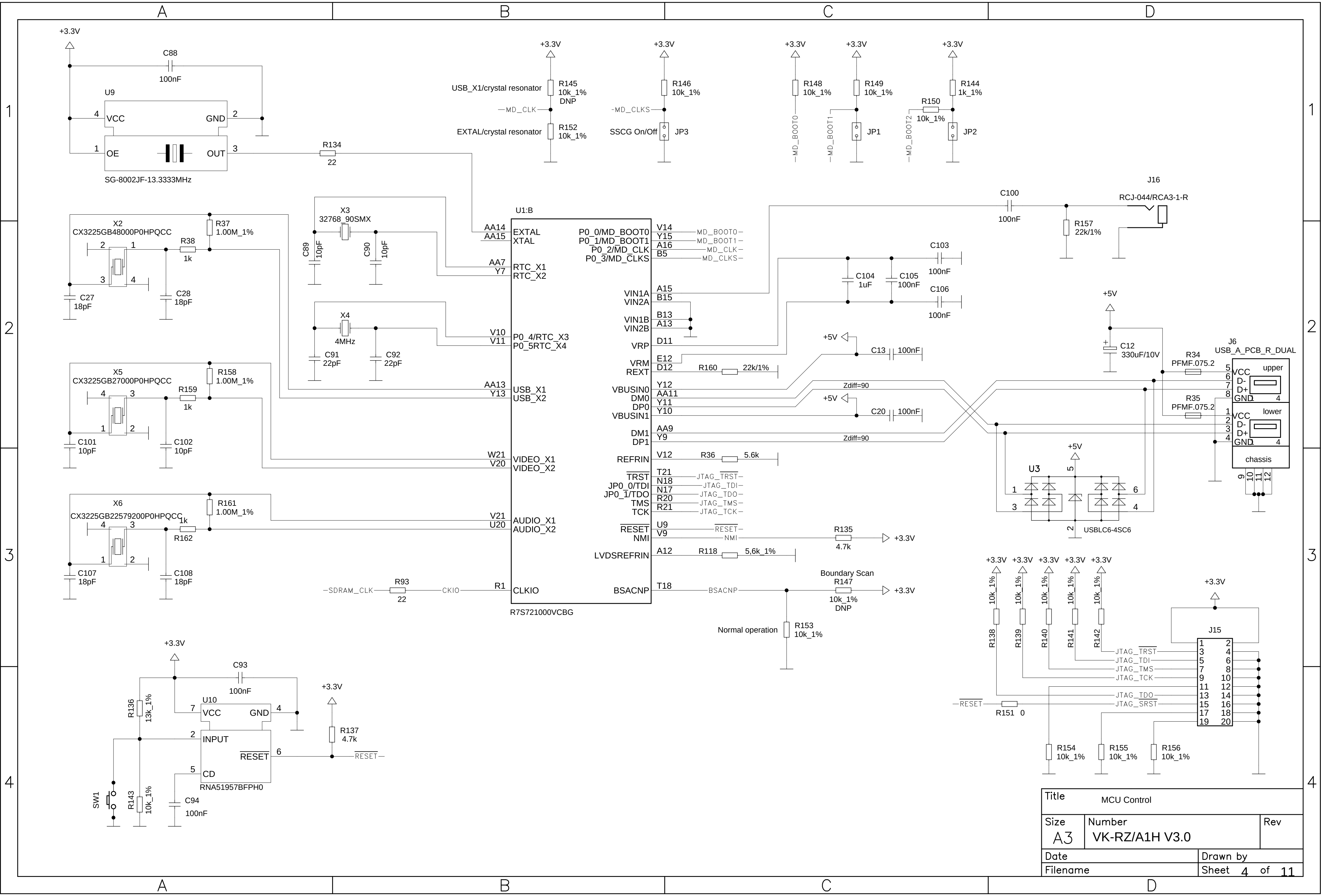
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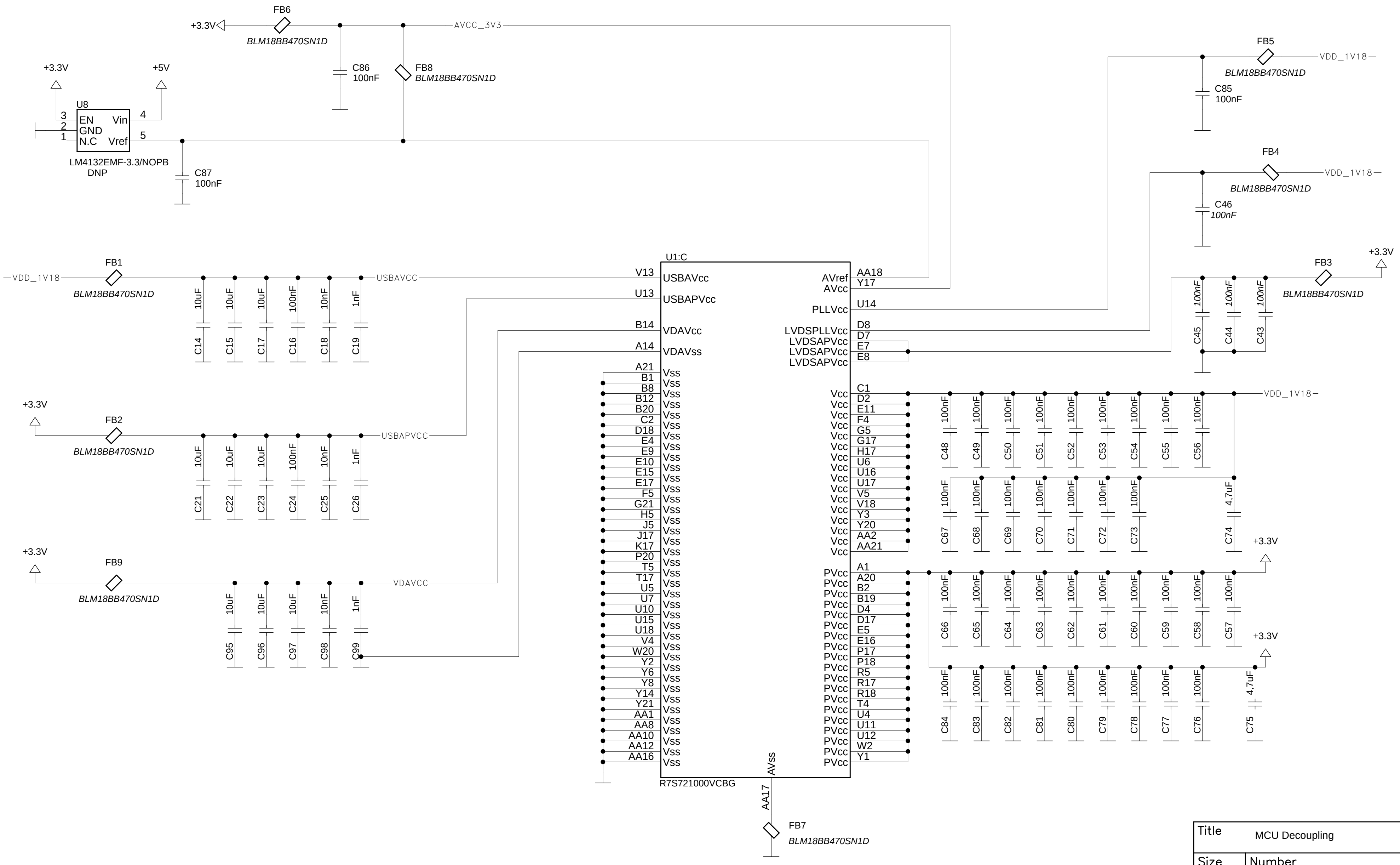
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Number	VK-RZ/A1H V3.0
Rev	
Date	
Drawn by	
Filename	
Sheet	2 of 11



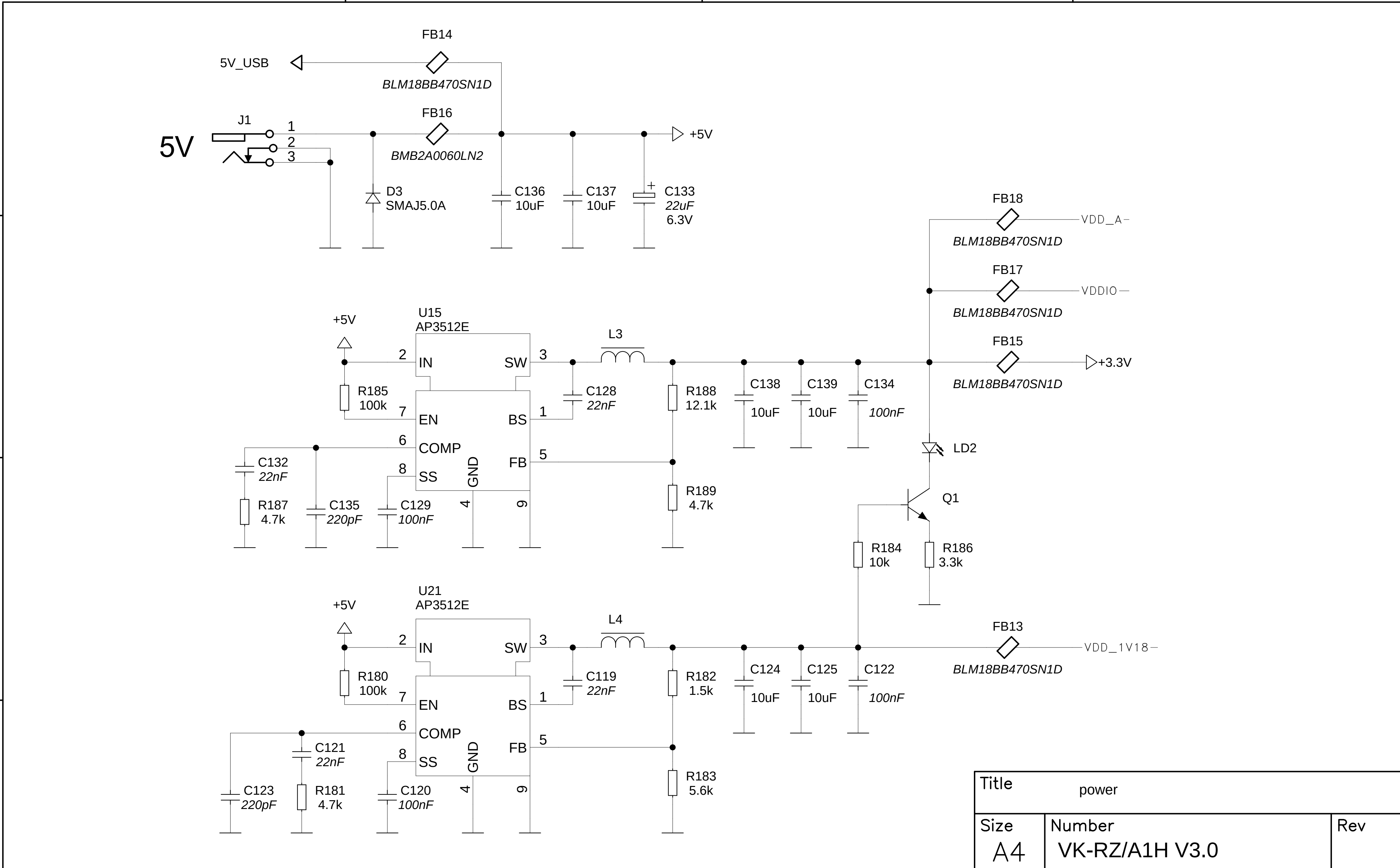
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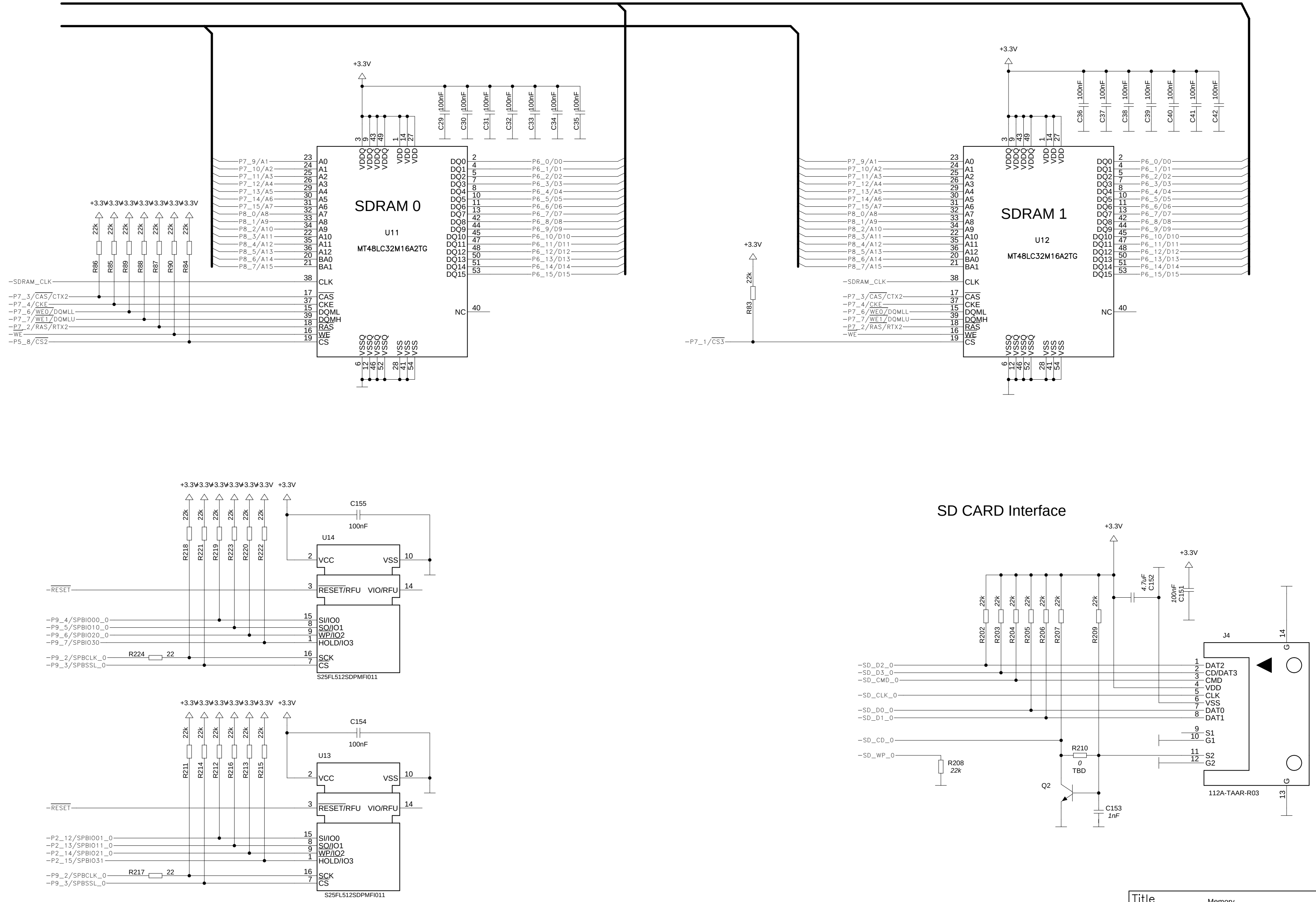
+3.3V
C88
100nF
U9
VCC
GND
OE
OUT
SG-8002JF-13.3333MHz
R134
22
USB_X1/crystal resonator
R145
10k_1%
DNP
MD_CLK
EXTAL/crystal resonator
R152
10k_1%
R146
10k_1%
MD_CLKS
SSCG On/Off
JP3
R148
10k_1%
R149
10k_1%
R144
1k_1%
R150
10k_1%
MD_BOOT0
MD_BOOT1
MD_BOOT2
JP1
JP2
J16
RCJ-044/RCA3-1-R
C100
100nF
R157
22k/1%
X2
CX3225GB48000P0HPQCC
R37
1.00M_1%
R38
1k
C27
18pF
C28
18pF
X3
32768_90SMX
C89
10pF
C90
10pF
U1:B
EXTAL
XTAL
RTC_X1
RTC_X2
P0_0/MD_BOOT0
P0_1/MD_BOOT1
P0_2/MD_CLK
P0_3/MD_CLKS
VIN1A
VIN2A
VIN1B
VIN2B
VRP
VRM
REXT
C103
100nF
C104
1uF
C105
100nF
C106
100nF
X4
4MHz
C91
22pF
C92
22pF
P0_4/RTC_X3
P0_5RTC_X4
+5V
C12
330uF/10V
J6
USB_A_PCB_R_DUAL
R34
PFMF.075.2
R35
PFMF.075.2
upper
lower
chassis
C13
100nF
C20
100nF
R160
22k/1%
Zdiff=90
X5
CX3225GB27000P0HPQCC
R158
1.00M_1%
R159
1k
C101
10pF
C102
10pF
USB_X1
USB_X2
VBUSIN0
DM0
DP0
VBUSIN1
DM1
DP1
VIDEO_X1
VIDEO_X2
REFRIN
R36
5.6k
U3
USBLC6-4SC6
TRST
JP0_0/TDI
JP0_1/TDO
TMS
TCK
JTAG_TRST
JTAG_TDI
JTAG_TDO
JTAG_TMS
JTAG_TCK
X6
CX3225GB22579200P0HPQCC
R161
1.00M_1%
R162
1k
C107
18pF
C108
18pF
AUDIO_X1
AUDIO_X2
RESET
NMI
R135
4.7k
LVDSREFRIN
R118
5.6k_1%
SDRAM_CLK
R93
22
CKIO
CLKIO
BSACNP
Boundary Scan
R147
10k_1%
DNP
R7S721000VCBG
Normal operation
R153
10k_1%
R138
R139
R140
R141
R142
10k_1%
J15
JTAG_SRST
R151 0
R154
10k_1%
R155
10k_1%
R156
10k_1%
C93
100nF
U10
INPUT
CD
RNA51957BFPH0
R136
13k_1%
R137
4.7k
R143
10k_1%
SW1
C94
100nF
Title MCU Control
Size A3
Number VK-RZ/A1H V3.0
Rev
Date
Drawn by
Filename
Sheet 4 of 11



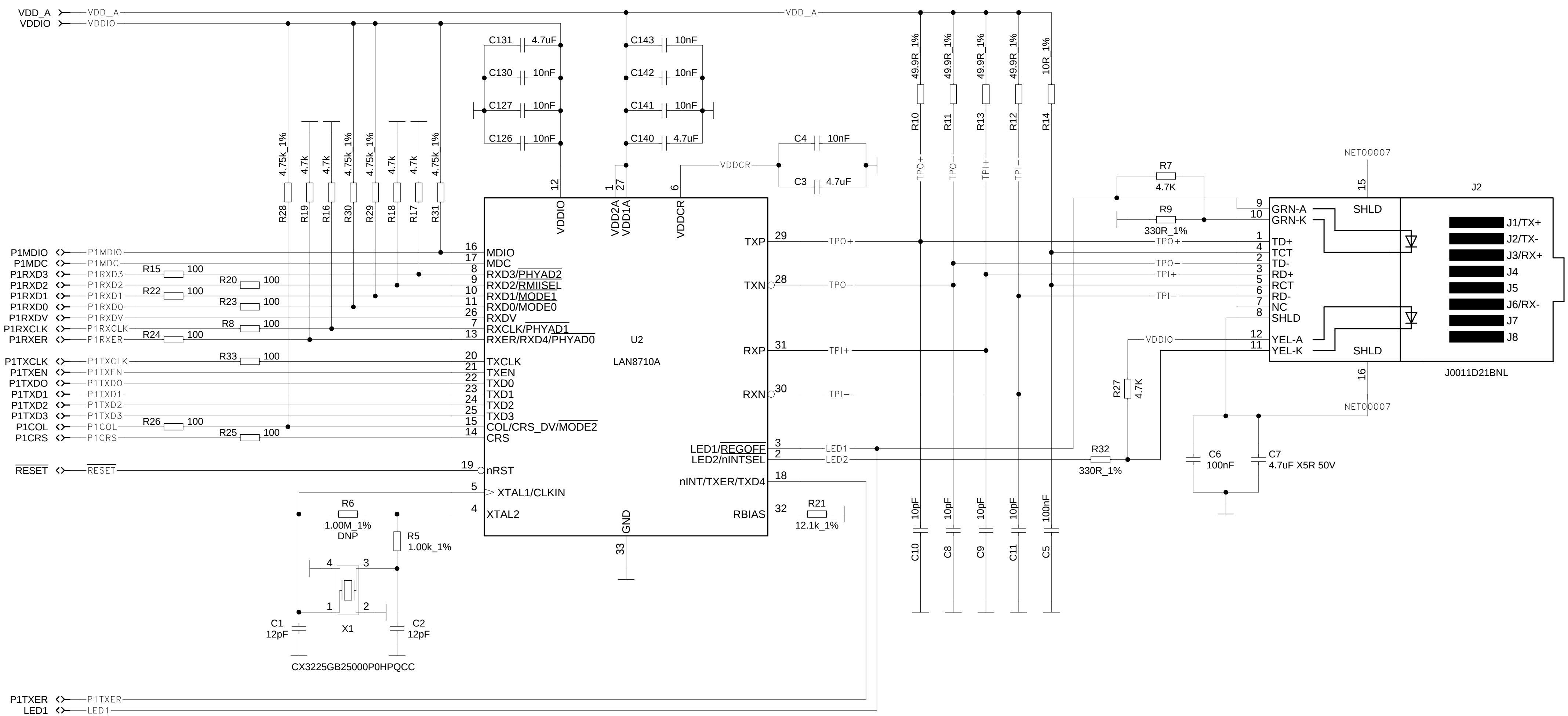
Title	MCU Decoupling
Size	A3
Number	VK-RZ/A1H V3.0
Rev	
Date	
Drawn by	
Filename	
Sheet	5 of 11



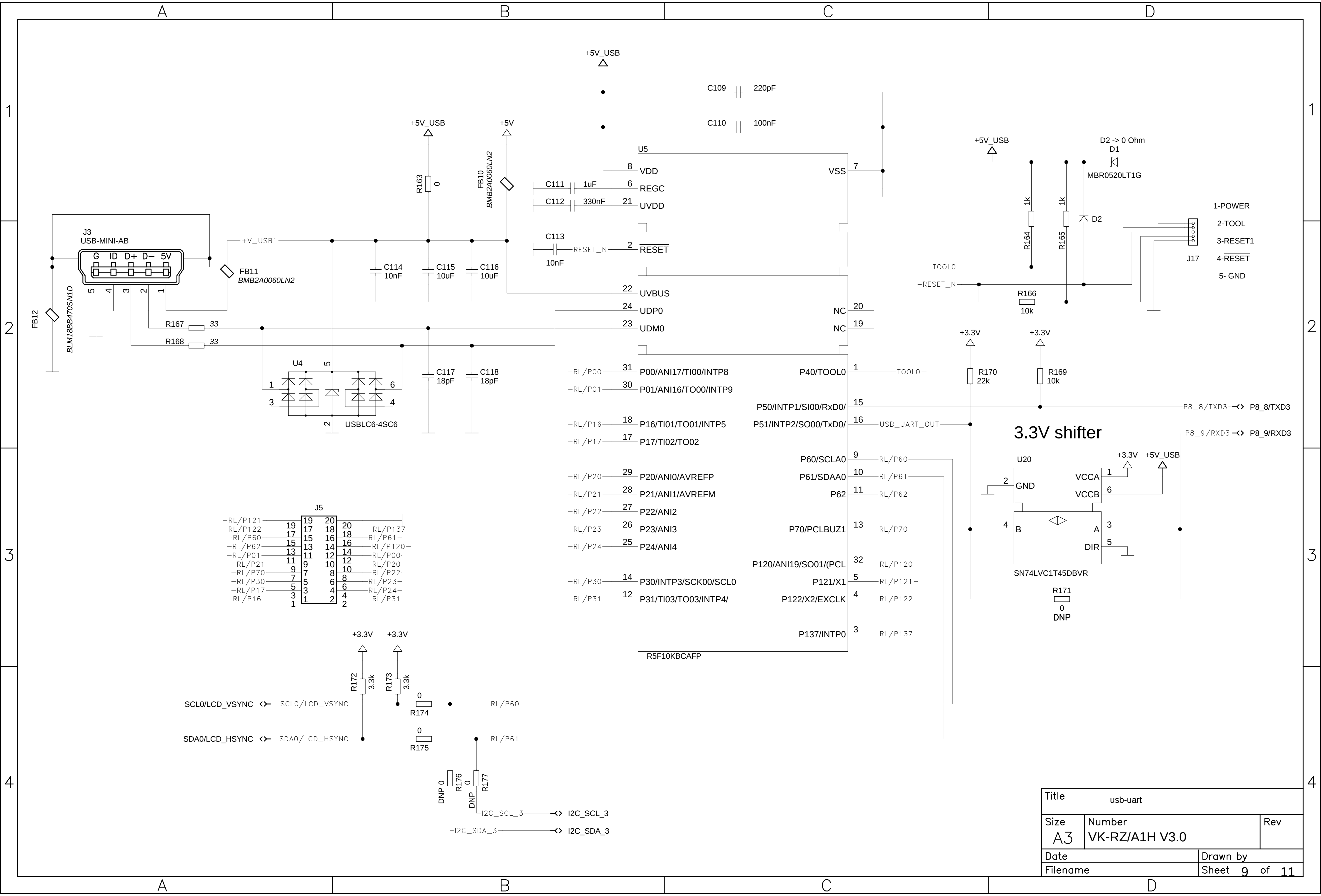
Title power		
Size A4	Number VK-RZ/A1H V3.0	Rev
Date	Drawn by	
Filename	Sheet 6 of 11	



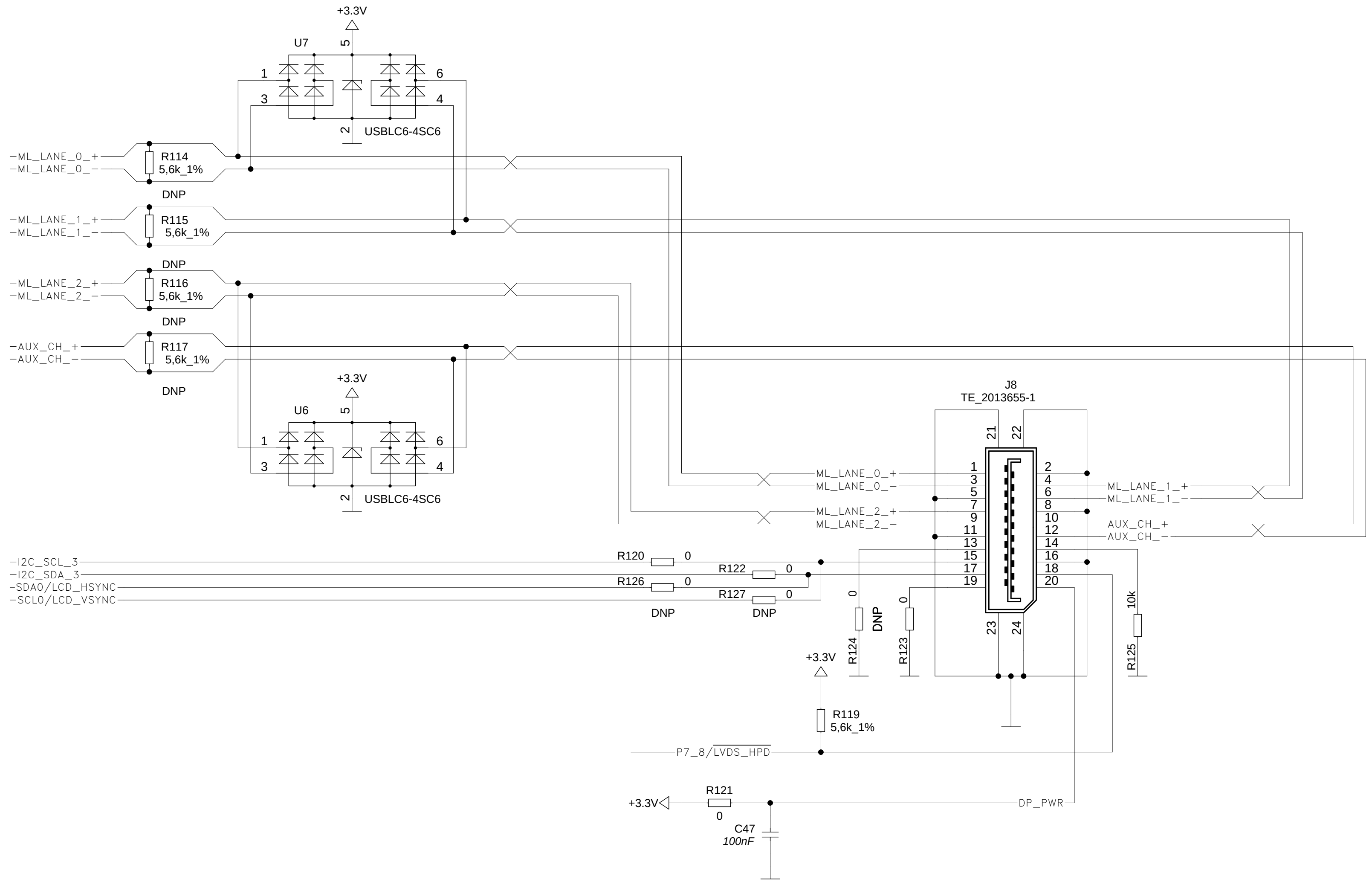
Title	Memory	
Size A2	Number VK-RZ/A1H V3.0	Rev
Date		Drawn by
Filename		Sheet 7 of 11



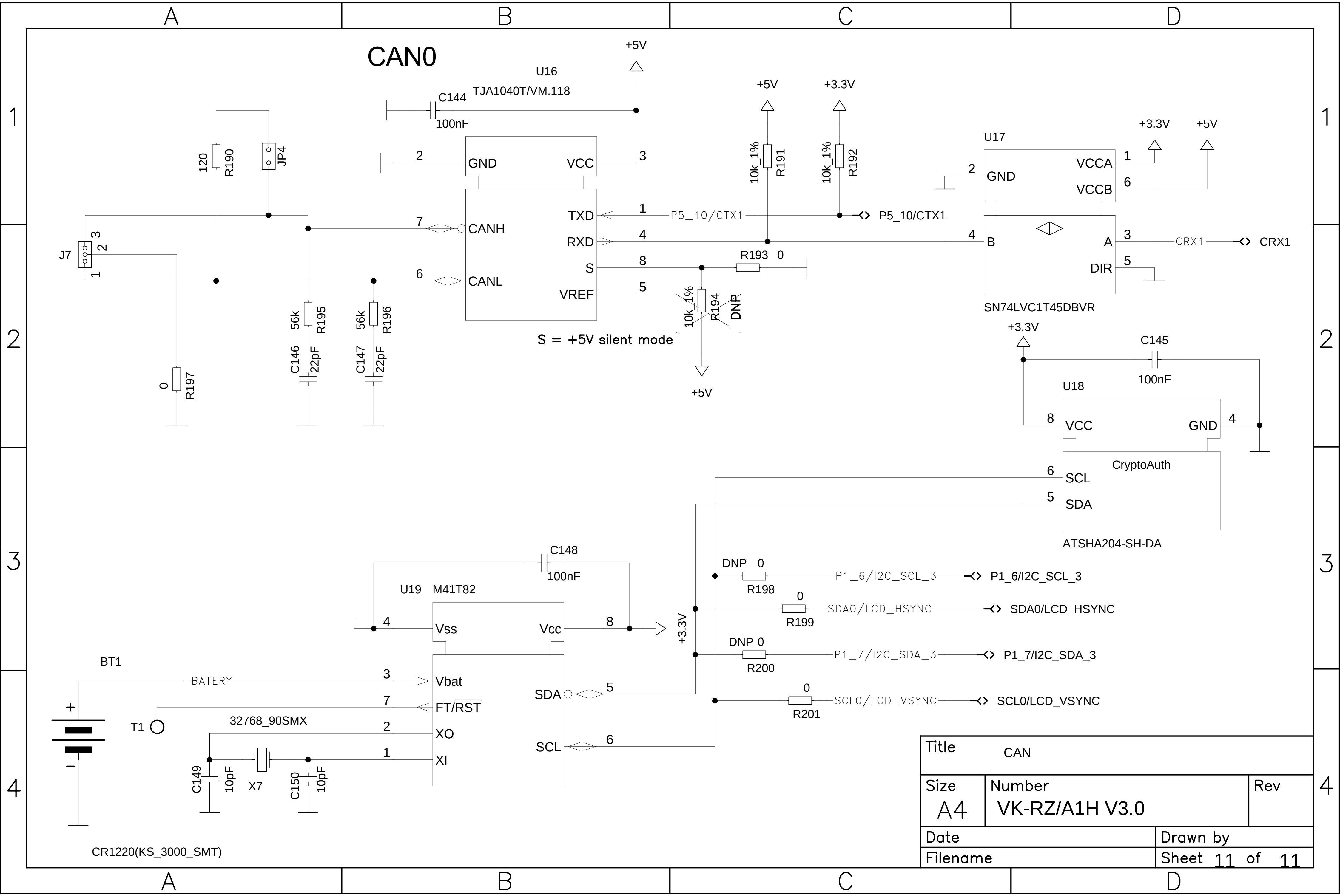
Title	LAN
Size	A3
Number	VK-RZ/A1H V3.0
Rev	
Date	
Drawn by	
Filename	VK_RZ_A1H_v3.sch
Sheet	8 of 11

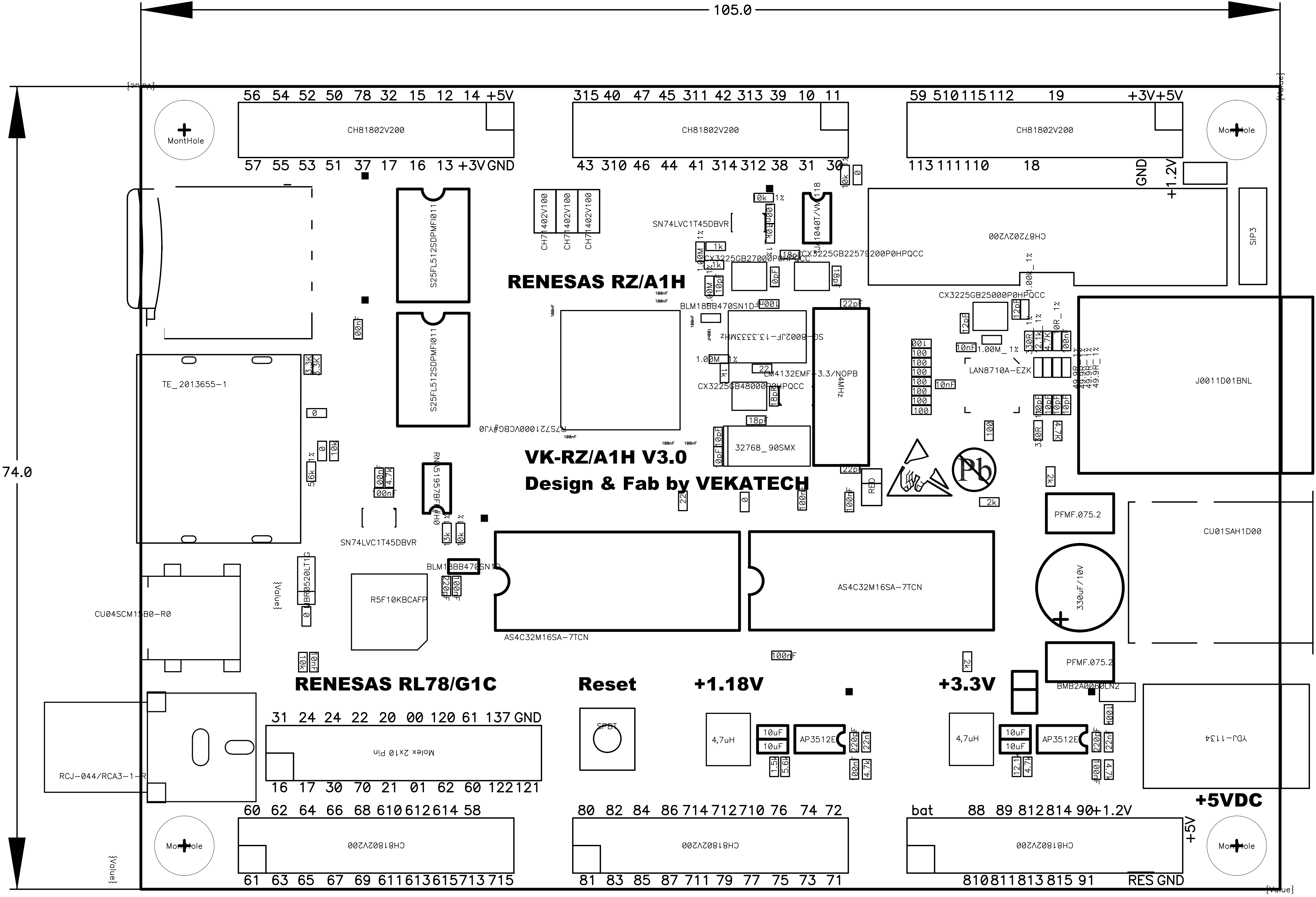


+5V_USB
C109 220pF
C110 100nF
+5V
R163 0
FB10 BMB2A0060LN2
U5
VDD
VSS
C111 1uF REGC
C112 330nF UVDD
C113 10nF RESET_N RESET
J3 USB-MINI-AB
G ID D+ D− 5V
+V_USB1
FB11 BMB2A0060LN2
C114 10nF
C115 10uF
C116 10uF
UVBUS
UDP0
UDM0
NC
NC
FB12 BLM18BB470SN1D
R167 33
R168 33
U4 USBLC6-4SC6
C117 18pF
C118 18pF
D2 -> 0 Ohm
D1 MBR0520LT1G
R164 1k
R165 1k
D2
1-POWER
2-TOOL
3-RESET1
4-RESET
5- GND
J17
TOOL0
RESET_N
R166 10k
+3.3V
R170 22k
R169 10k
P00/ANI17/TI00/INTP8
P01/ANI16/TO00/INTP9
P16/TI01/TO01/INTP5
P17/TI02/TO02
P20/ANI0/AVREFP
P21/ANI1/AVREFM
P22/ANI2
P23/ANI3
P24/ANI4
P30/INTP3/SCK00/SCL0
P31/TI03/TO03/INTP4/
P40/TOOL0
P50/INTP1/SI00/RxD0/
P51/INTP2/SO00/TxD0/
P60/SCLA0
P61/SDAA0
P62
P70/PCLBUZ1
P120/ANI19/SO01/(PCL
P121/X1
P122/X2/EXCLK
P137/INTP0
R5F10KBCAFP
P8_8/TXD3
P8_9/RXD3
USB_UART_OUT
3.3V shifter
U20
GND
VCCA
VCCB
B
A
DIR
SN74LVC1T45DBVR
R171 0 DNP
J5
R172 3.3k
R173 3.3k
R174 0
R175 0
SCL0/LCD_VSYNC
SDA0/LCD_HSYNC
RL/P60
RL/P61
R176 0 DNP
R177 0 DNP
I2C_SCL_3
I2C_SDA_3
Title usb-uart
Size A3
Number VK-RZ/A1H V3.0
Rev
Date
Drawn by
Filename
Sheet 9 of 11

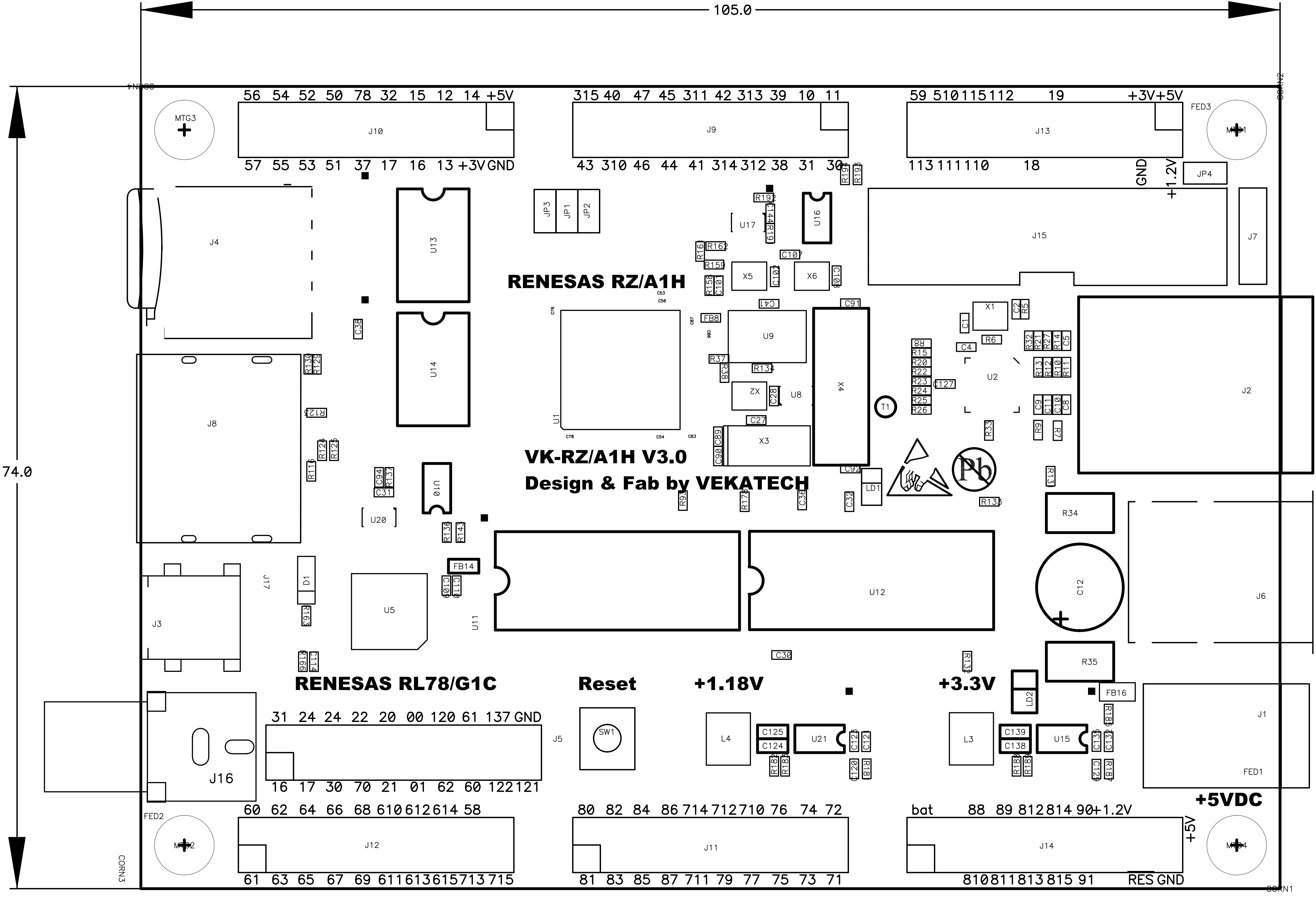


Title	Display	
Size A3	Number VK-RZ/A1H V3.0	Rev
Date	Drawn by	
Filename	Sheet 10 of 11	

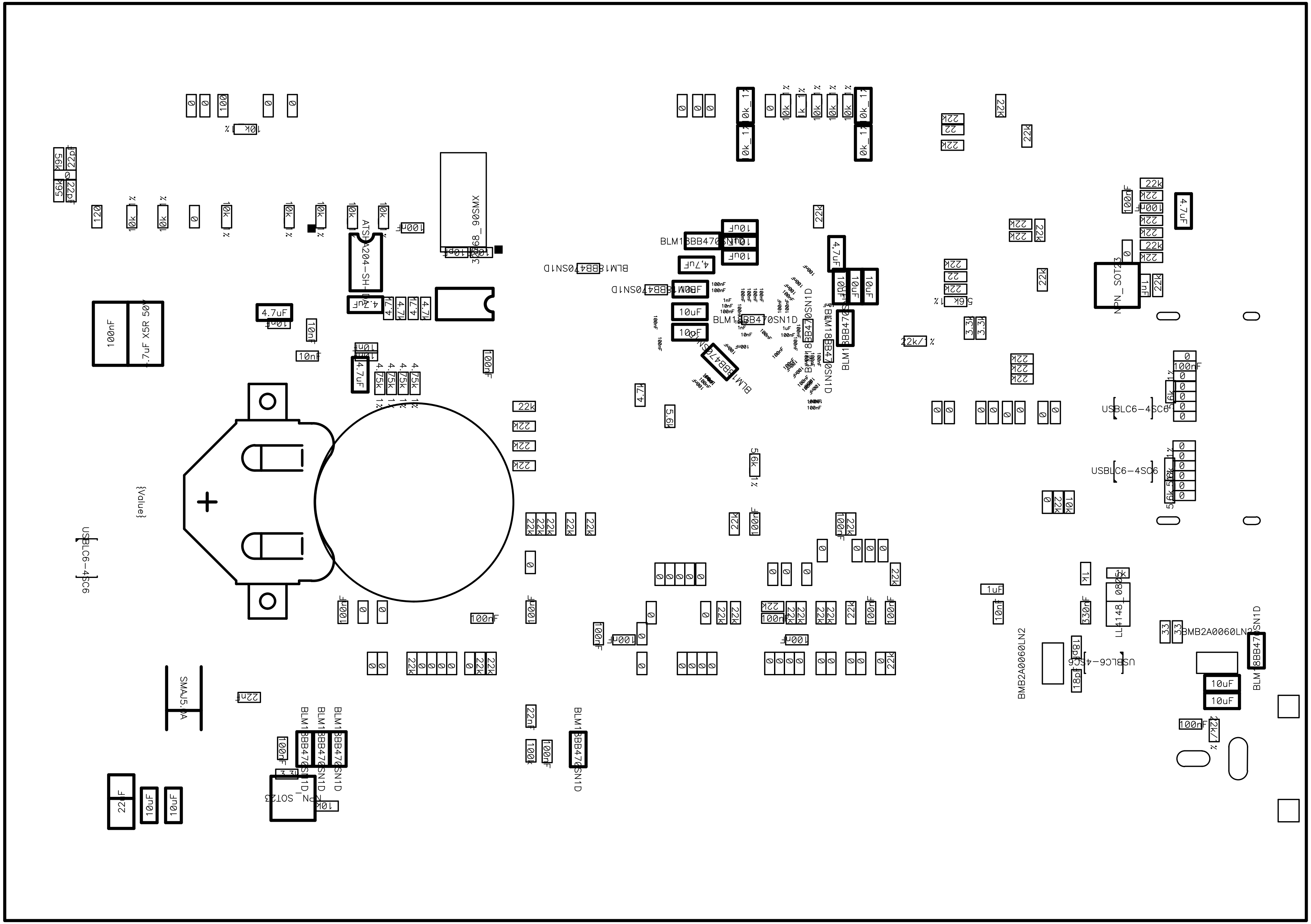

CAN0
U16
TJA1040T/VM.118
+5V
C144
100nF
GND
VCC
CANH
CANL
TXD
RXD
S
VREF
120
R190
JP4
J7
0
R197
56k
R195
56k
R196
C146
22pF
C147
22pF
P5_10/CTX1
R193 0
10k_1%
R194
DNP
S = +5V silent mode
+3.3V
10k_1%
R191
10k_1%
R192
U17
VCCA
VCCB
B
A
DIR
SN74LVC1T45DBVR
CRX1
C145
100nF
U18
VCC
CryptoAuth
SCL
SDA
ATSHA204-SH-DA
C148
100nF
U19
M41T82
Vss
Vcc
Vbat
FT/RST
XO
XI
SDA
SCL
BT1
BATERY
T1
32768_90SMX
C149
10pF
X7
C150
10pF
CR1220(KS_3000_SMT)
DNP 0
R198
P1_6/I2C_SCL_3
0
R199
SDA0/LCD_HSYNC
DNP 0
R200
P1_7/I2C_SDA_3
0
R201
SCL0/LCD_VSYNC
A
B
C
D
1
2
3
4
Title
CAN
Size
A4
Number
VK-RZ/A1H V3.0
Rev
Date
Drawn by
Filename
Sheet 11 of 11

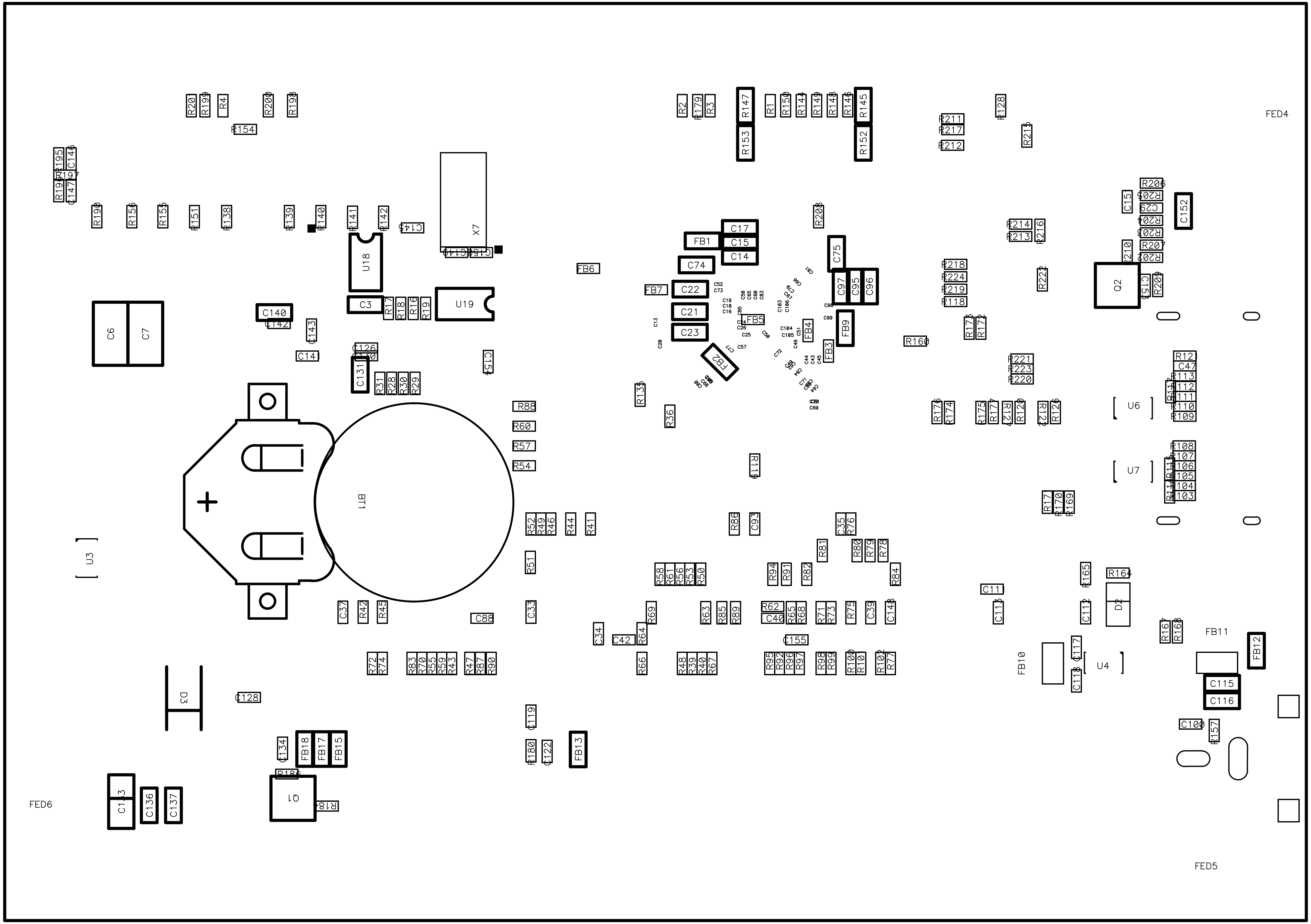


VK_RZ_A1H_v3_0_revA_16_7_15



VK_RZ_A1H_v3_0_revA_16_7_15


BLM18BB470SN1D
ATSHA204-SH-DA
USBLC6-4SC6
SMAJ5.0A
NPN_SOT23
BMB2A0060LN2
LL4148_080
4.7uF
10uF
100nF
22k
{Value}



FED4
FED5
FED6
R20
R199
R4
R200
R198
R154
R195
C146
R197
R196
C147
R190
R156
R155
R151
R138
R139
R140
R141
R142
C145
X7
U18
U19
C3
R17
R18
R16
R19
C6
C7
C140
C142
C143
C14
C126
C131
R31
R28
R30
R29
C154
BT1
R88
R60
R57
R54
U3
D3
C128
C134
FB18
FB17
FB15
R186
Q1
R184
C133
C136
C137
C37
R42
R45
C88
R72
R74
R83
R70
R55
R59
R43
R47
R87
R90
R52
R49
R46
R44
R41
R51
C33
C119
R180
C122
FB13
FB6
R2
R179
R3
R147
R153
R1
R150
R144
R149
R148
R146
R145
R152
R208
C17
FB1
C15
C14
C74
C75
C22
FB7
C21
C23
FB5
FB4
FB3
FB2
FB9
C97
C95
C96
R135
R36
R119
R86
C93
C35
R76
R81
R80
R79
R78
R58
R61
R56
R53
R50
R94
R91
R82
R84
R69
R64
C34
C42
R66
R63
R85
R89
R62
C40
R65
R68
R71
R73
R75
C39
C148
C155
R48
R39
R40
R67
R95
R92
R96
R97
R98
R99
R100
R10
R102
R77
R211
R217
R212
R128
R215
R214
R213
R216
R218
R224
R219
R118
R222
R160
R221
R223
R220
R176
R174
R175
R177
R120
R126
R206
C152
R207
R202
R210
Q2
R209
U6
U7
R108
R107
R106
R105
R104
R103
R109
R110
R111
R112
R113
C47
R170
R169
C111
C113
R165
R164
D2
C112
C117
C118
U4
FB10
FB11
FB12
R167
R168
C115
C116
C100
R157